ABSTRACT OF THE DISCLOSURE

An operation method for non-volatile memory is conducted as follows. First, a non-volatile memory cell capable of storing a first bit and a second bit is provided. The non-volatile memory cell comprises a first region and a second region with a channel therebetween and a gate above the channel but separated therefrom by a charge trapping layer, wherein the first bit and the second bit are positioned close to the first and second regions, respectively. Next, a first programmed voltage for the first bit, a second programmed voltage for the second bit and an erased voltage for the first and second bits are determined, wherein the first programmed voltage is smaller than the second programmed voltage. For reading the first bit, a voltage is applied to the second region, inducing a depletion region around the second region. For reading the second bit, a voltage is applied to the second region, wherein the voltage applied to the second region is smaller than that for reading the first bit.